



Radiation Testing, Characterization and Qualification Challenges for Modern Microelectronics and Photonics Devices and Technologies

Kenneth A. LaBel

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Lewis M. Cohn, Defense Threat Reduction Agency

To be presented by Kenneth A. LaBel at the Government Microcircuit Applications & Critical Technology Conference (GOMAC), March 17-20, 2008, Las Vegas, NV.



Outline of Presentation

- **Introduction**
- **Single Event Effect (SEE) Testing and Complex Device Packages**
 - Packaging material
 - Thermal control
 - Particle interarrival angle
 - The direction the particle enters the device
- **SEE Sensitive Devices**
 - Optical devices and the increased sensitivity of CMOS
 - Changing the way we test and predict space performance
- **The Impact of System-on-a-Chip (SOC) Device Complexity**
 - Example: Field Programmable Gate Array (FPGA) complexity
 - Fault Isolation
 - Data Interpretation
 - Statistical Data Gathering
 - Total Ionizing dose (TID) test logistics
- **Considerations**

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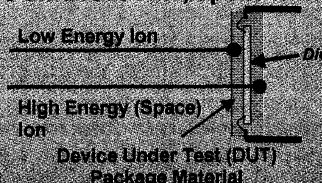
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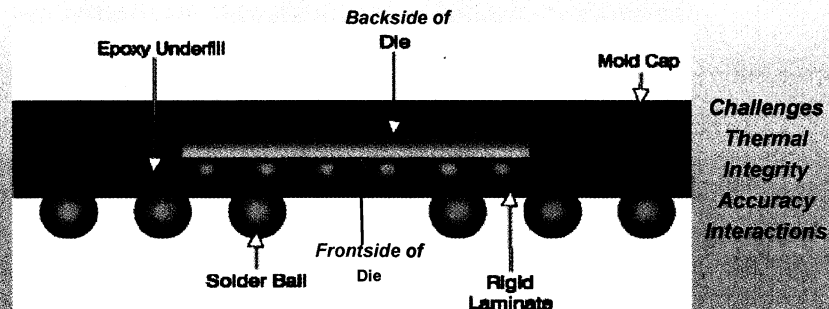
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Device Package and Particle Penetration – Example: Flip-Chip Ball Grid Array (FBGA)



Must remove sufficient amount of material to
penetrate to backside of die AND
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Challenges
Thermal
Integrity
Accuracy
Interactions

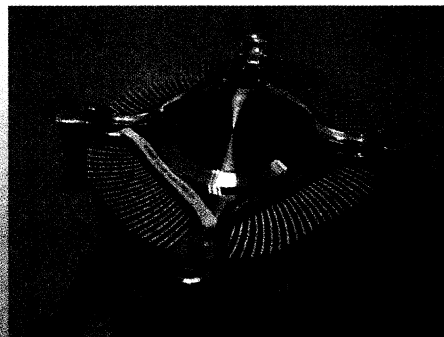
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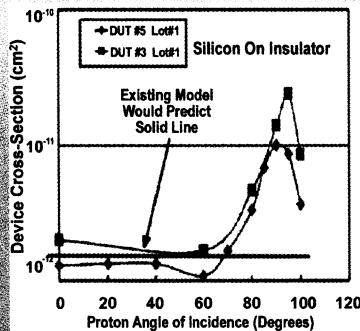
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Simulating the Space Environment



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 - Part is usually tilted to simulate angular space effects
- The underlying assumption is often false



Challenges

Tilting part =
Increasing path through device
(Ion range limitation)

Asymmetry of transistors =
Test in both tilt axes PLUS
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Backside/frontside =
Impossible to perform without major effort

Modeling =
Hard to model w/o detailed
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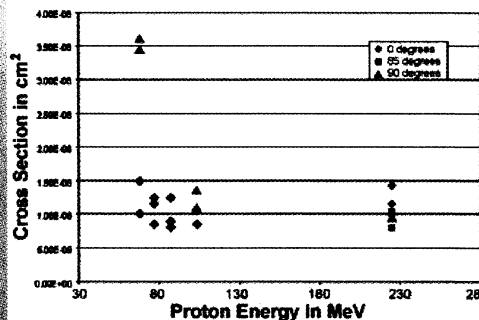
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Are We Approaching a Meltdown?



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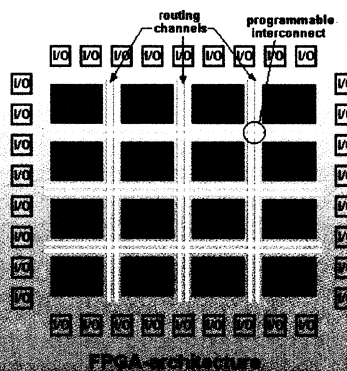
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 - Cell spacing (multi-bit upsets or MBUs) or
 - Operating speed (SEU event may last longer than one clock period),
 - Software interrupts, and more
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How is SRAM-like
configuration memory like
an umbrella?

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 - Understanding what within the device is causing an event.
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 - Other tools, such as two photon absorption (TPA) lasers may also be useful
 - Beware: SOC's are usually in packages such as FBGAs and the challenges discussed earlier play into this discussion as well.
 - Device complexity does not lead to full silicon testability
 - Errors can be masked (i.e., hit to configuration may mask state machine errors)
 - Hidden registers
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- What does this imply? Is all existing SOC test data useless?
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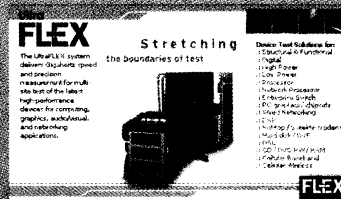
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Considerations



- We have discussed just a few of the emerging challenges related to modern radiation effects testing
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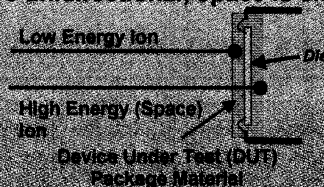


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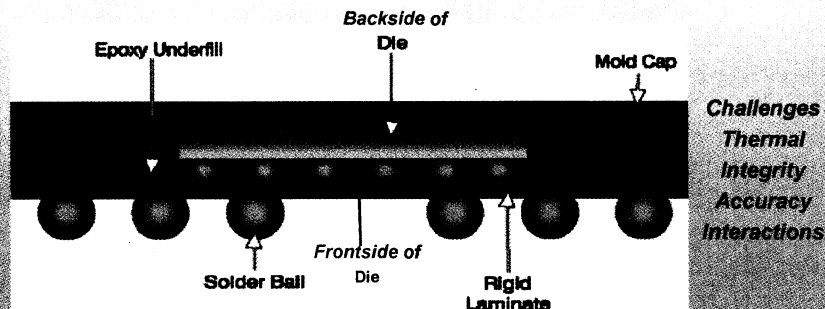


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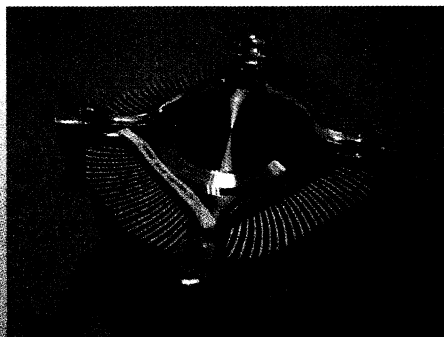
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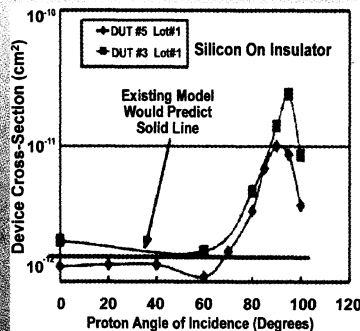
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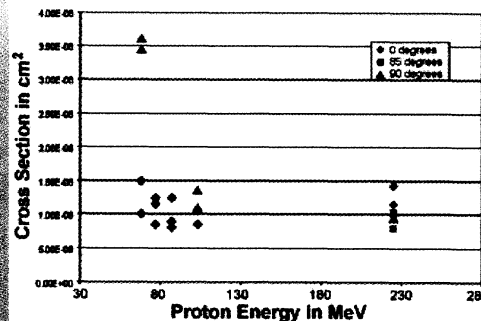
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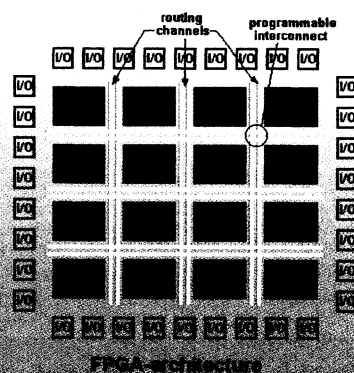
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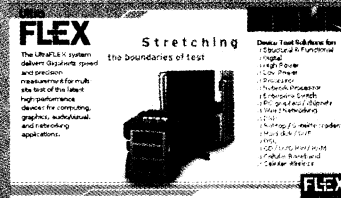
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